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ARCHITECTURE ANALYSIS OF HIGH PERFORMANCE CAPACITORS (POSTPRINT)

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14. ABSTRACT
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Architecture Analysis of High Performance Capacitors

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Abstract

Evolutionary increases in the demand on electrical power systems have resulted in the need to develop the next generation of compact, power dense, electrical systems utilizing robust and efficient high voltage power devices that are operable over an extended temperature range (-55°C to 250°C). In particular, there is a need to investigate novel capacitive architectures as a means to compliment recent advances in SiC power devices and high temperature magnetic and insulation materials. These advanced electrical components have enabled the demonstration of compact, high switch rate power system components that can operate at temperatures in excess of 200°C, but have been limited by current capacitor technology. Of concern with present state of the art capacitors are their volumetric energy density, dissipation factor, thermal stability, parasitic inductance, and failure mechanisms. A modeling and simulation capability will be described herein, which was used to investigate device architecture-electrical performance relationships for wound, collapsed, and stacked devices. Initially, a mathematical model is developed and utilized for both equivalent capacitor circuit analysis and device architecture field analysis, which were then used to identify factors (e.g., electrode, dielectric, contacts, etc.) that affect ESR, ESL, and capacitance. Additionally, finite element analysis of selected device architectures was accomplished to compare magnetic fields and thermal profiles predicted. The predicted electrical properties resulting from these analyses were then utilized as SPICE simulation input parameters to evaluate the performance of the different capacitors in a dc-dc boost converter model. Finally, modeling and simulation results are compared to empirical data sheet information and experimental data. The knowledge gained from this study provides insight into the key capacitor design and packaging parameters yielding optimized voltage, current, DF, and frequency characteristics for designated applications.

Key words: Capacitor architecture, ESR, ESL, FPE, Voltage ripple, DC/DC converter

I. Introduction

Throughout aviation history, aircraft electrical systems have consistently evolved into higher power, more compact architectures as a means to increase flight performance (e.g., thrust and maneuverability) and enhance onboard mission capability (e.g., sensors, weapons, communications) [1]. Recently, there has been a concerted effort in the aviation community to develop "more electric" architectures as a means to improve the capability, reliability, and maintainability of these systems [2]. As these electrical systems have matured, thermal management requirements have become challenging,

due to contradictory effects of using higher power/thrust, increased power density, and reduced heat sink capability. One approach is to develop high temperature, efficient power conditioning systems to reduce the thermal load to the heat pump and/or to enable placement of electrical technology in close proximity to heat sources (e.g., generators, motors, leading).

Capacitors are a critical component in the design of advanced power conditioning systems (e.g., converters, inverters) and are commonly identified as the lease mature technology with respect to volumetric energy density, operational temperature range, and manufacturing cost [3]. In addition, the interest in raising the upper temperature limit for capacitors has grown due to recent progress in silicon carbide technology [4], high-temperature magnetic material [5], and the demonstration of these components into power electronics for operation at temperatures above 200°C [6]. Candidate capacitors include a variety of ceramic-type devices [7, 8], as well as efforts to develop high-temperature polymer film capacitors [9] or stacked inorganic thin film capacitors [10, 11]. While these efforts focus on utilizing thermally stable, high-energy density dielectric materials, little attention has been dedicated to addressing whether they can be packaged in a manner that fulfills all of the encompassing capacitor performance requirements (e.g., ESR, ESL, efficiency, internal heating).

The study presented herein is part of a larger effort to establish a better understanding of how to incorporate advanced materials into appropriate device architectures so as to fulfill the requirements identified for targeted applications (e.g., voltage stabilization, power factor correction, and frequency filtering). This knowledge can then be applied to identify whether requirements such as voltage breakdown strength, energy density, and graceful failure can be obtained while still maintaining a low equivalent series resistance and inductance. This knowledge base is also applicable to other requirements such as low heat dissipation, high ripple current, high frequency, and combinations thereof. These considerations require an in-depth analysis of the capacitor architecture to include material components and their respective thickness since it is expected to have a notable impact on the device performance and therefore limit its potential application [12], [13].

In this study, an analysis of the capacitor architecture is conducted with modeling, simulation, and empirical data compared. Modeling techniques are utilized to gain a better understanding of the components in an equivalent circuit for a capacitor, which are then incorporated into simulations generated with finite element method software. The simulations are used to evaluate the magnetic fields and thermal profile for stacked and wound (collapsed and cylindrical) capacitor architectures as a means to study the parasitic inductance and heat dissipation. A combination of the modeling and simulation results are then correlated with empirical data obtained from commercially available capacitors, which includes the measurement of heat dissipated from a recently developed fluorenyl polyester (FPE) capacitor under an AC excitation.

II. Capacitor Modeling for ESR and DF

By solving the capacitor equivalent circuit model shown in Figure 1, the equivalent series resistance (ESR) and dissipation factor (DF) can be derived.

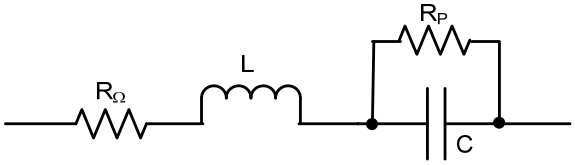


Figure 1: Equivalent circuit model of a capacitor.

In the above model, R_P represents the dielectric and absorption loss and R_Ω represents the ohmic loss. The ohmic losses are contributed by electrode resistance as well as various manufacturing-specific resistances such as interface resistance between the electrodes and dielectric, solder termination resistance, lead resistance, and resistive loss due to fringing field from the dielectric. From this circuit model, the total circuit impedance (Z_{cap}) is expressed in equations (1) and (2).

$$Z_{cap} = R_\Omega + j\omega L + \frac{1}{\frac{1}{R_P} + j\omega C} \quad (1)$$

$$Z_{cap} = \left(R_\Omega + \frac{R_P}{1+\omega^2 C^2 R_P^2}\right) + j\left(\omega L - \frac{\omega C R_P^2}{1+\omega^2 C^2 R_P^2}\right) \quad (2)$$

Using (2), expressions for ESR and DF are then defined.

$$ESR = R_\Omega + \frac{R_P}{1+\omega^2 C^2 R_P^2} \quad (3)$$

$$DF = \frac{|ESR|}{|X|} = \frac{\left|R_\Omega + \frac{R_P}{1+\omega^2 C^2 R_P^2}\right|}{\left|\omega L - \frac{\omega C R_P^2}{1+\omega^2 C^2 R_P^2}\right|} \quad (4)$$

If $|\omega L| << \left|\frac{\omega C R p^2}{1+\omega^2 C^2 R p^2}\right|$, then

$$DF = \frac{\left|R_\Omega + \frac{Rp}{1+\omega^2 C^2 Rp^2}\right|}{\left|-\frac{\omega C R p^2}{1+\omega^2 C^2 Rp^2}\right|} = \frac{\left|R_\Omega(1+\omega^2 C^2 Rp^2) + Rp\right|}{\left|-\omega C R p^2\right|} \quad (5)$$

Since $R_\Omega << Rp$, DF becomes

$$DF = \frac{1}{\omega C R_P} + \omega C R_\Omega \quad (6)$$

Assuming C is very close to a constant value over the range of 20 Hz to 1 MHz, the first term of (6) dominates the dissipation factor at low frequencies, while at high frequencies the second term becomes the dominant factor [14]. Further, for a capacitor with very low dielectric loss corresponding to a very high value of R_P, the ESR and DF become the familiar expressions under ideal conditions given by (7) and (8).

$$ESR = R_\Omega \quad (7)$$

$$DF = \omega C R_\Omega \quad (8)$$

III. Capacitor Architecture Study

In order to evaluate the relationship between capacitor architecture and its electrical and thermal performance, the following four architectures were considered: collapsed, stacked, cylindrical, and wider stacked. A 10 μF/100 V collapsed metallized polycarbonate capacitor [15] was used as the reference capacitor for this study. A pictorial view of the reference collapsed capacitor, with an external copper sheath as a low inductance return current path, is shown in Figure 2.

The surface outline diagram for the four capacitor architectures considered is shown in Figure 3, including that of the reference collapsed capacitor. The other three capacitor architectures were sized to maintain the cross-sectional area, depth, and volume that of the reference capacitor for the purpose of electrical and thermal performance comparisons. Initial finite element analysis simulation, using the software *QuickField Professional*, was accomplished to predict temperature distributions and parasitic inductance. The results of these simulations are shown in Table I. It was assumed that 1 W of power was dissipated in the capacitors and the equivalent thermal conductivity of the dielectric film was 0.2 W/mK. The data in Table I predicts that the peak temperature rise is lowest (4.63 K) for the wider stacked capacitor geometry, whereas the cylindrical and collapsed geometries show a maximum temperature rise of ~15 K. In terms of the equivalent series inductance (ESL), the wider stacked capacitor also provides a lower predicted ESL of 0.577 nH, whereas the collapsed and cylindrical geometries result in a predicted ESL in excess of 1.3 nH.

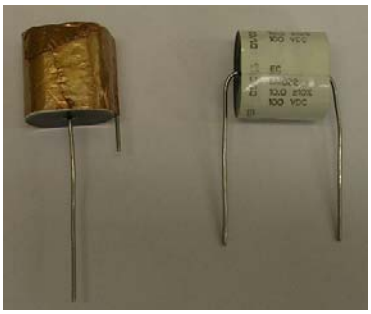


Figure 2: A pictorial view of the collapsed 10 μF metallized polycarbonate capacitor used as the reference capacitor for this study.

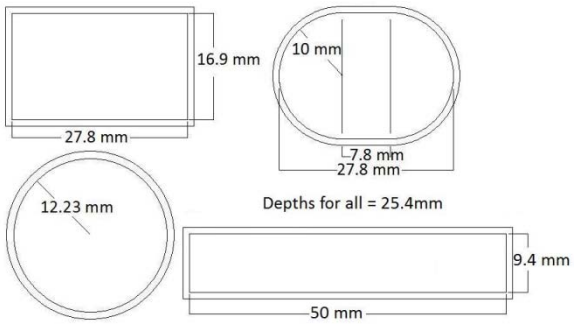
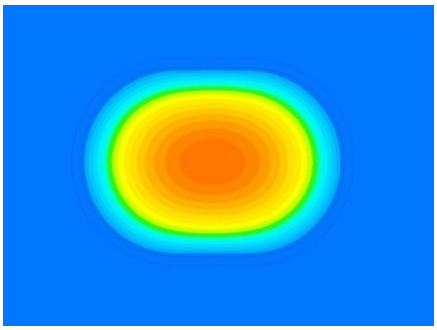


Figure 3: Capacitor architectures studied for electrical and thermal performance evaluation (Clockwise: Stacked, collapsed, wider stacked, and cylindrical)

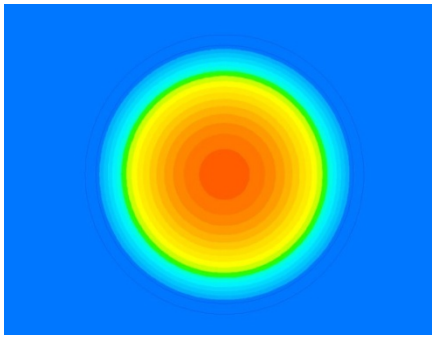
Table I: Summary of the finite element analysis results for the capacitor thermal and electrical performance

Capacitor Type	Collapsed capacitor	Stacked capacitor	Cylindrical capacitor	Wider stacked capacitor
Depth (mm)	25.4	25.4	25.4	25.4
Height (mm)	20	16.9		9.4
Width (mm)	27.8	27.8		50
Radius (mm)			12.23	
Cross Sectional Area (cm^2)	4.7	4.7	4.7	4.7
Power in (W)	1	1	1	1
Thermal Conductivity (W/mK)	0.2	0.2	0.2	0.2
Surface Temp (K)	300	300	300	300
Max Temp (K)	314.95	312.64	315.66	304.63
Inductance (nH)	1.327	1.254	1.369	0.577

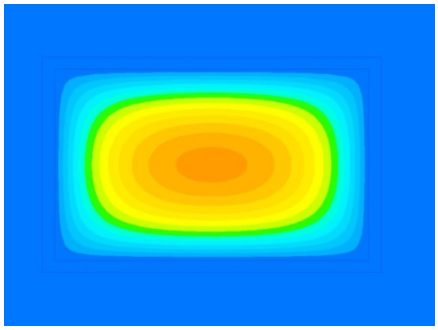
A comparison of the simulated temperature distributions among the four capacitors is shown in Figure 4. In addition to having the smallest maximum temperature rise of the four geometries, the wider stacked capacitor is seen to yield a lower temperature distribution throughout the entire device. This is a result of the wider stacked capacitor's larger surface area and shorter height. The heat, which is dissipated from the center, has less distance to travel to the surface. Conversely, the cylindrical capacitor presents more thermal resistance due to the larger radius and wound nature of the device. The distribution of flux density in the capacitors resulting from a simulated current of 1 A is shown in Figure 5. These devices have an outer layer, which represents a copper shroud that is wrapped around each device. The copper shroud is electrically connected to the device such that the current that goes into the device follows a path out through the shroud. This results in the magnetic field being essentially confined inside the capacitor. Interestingly, although the cylindrical capacitor had the highest inductance value, the collapsed capacitor appears to show the highest flux density values. For example, the maximum flux density value within the collapsed capacitor was recorded to be about 1.71×10^{-5} T; whereas the maximum flux density value in the cylindrical capacitor was about 1.60×10^{-5} T. Figure 5 shows this difference which is only about 6.6%. From the simulation results, it can be concluded that the wider stacked geometry is superior in terms of both ESL and temperature rise with respect to the collapsed and cylindrical geometries.



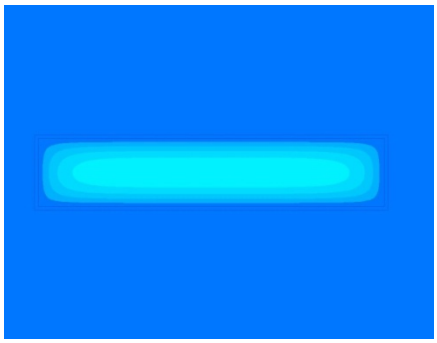
(a) Collapsed capacitor



(b) Cylindrical capacitor



(c) Stacked capacitor



(d) Wider stacked capacitor

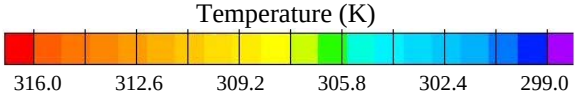
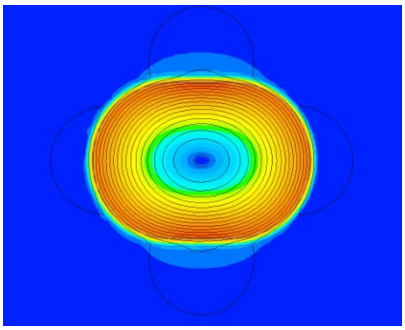
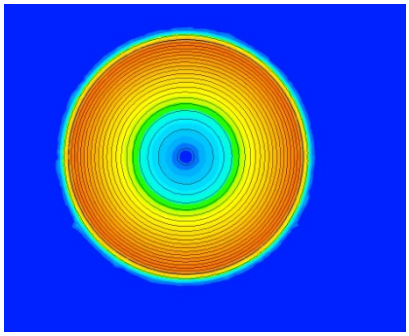


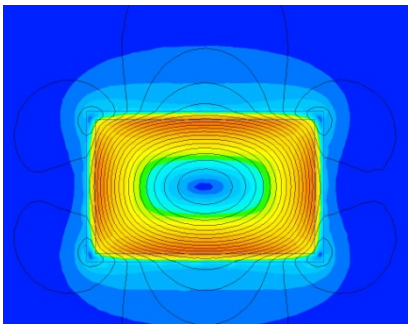
Figure 4: Temperature rise distribution for the four capacitor architectures dissipating 1 W of power.



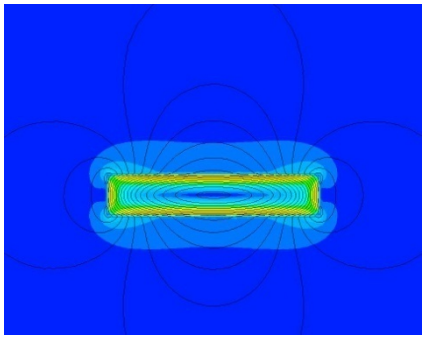
(a) Collapsed capacitor



(b) Cylindrical capacitor



(c) Stacked capacitor



(d) Wider stacked capacitor

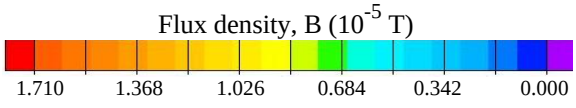


Figure 5: Magnetic field distribution for the four capacitor architectures carrying 1 A of current.

IV. Thermal and Electrical Performance of FPE Capacitors

A cylindrical 10 μF FPE metallized film capacitor was characterized in terms of electrical and thermal performance. FPE dielectric film has highly desirable properties including a stable dielectric constant over wide frequency (up to 1 MHz) and temperature (up to 250°C) ranges [9]. Recently, FPE capacitors passed lifetime tests of 250 hours at 200°C and 250 VDC, demonstrating their ability to withstand high voltage and temperature conditions. Figure 6 shows a packaged as well as an unpackaged FPE capacitor used in this study. The diameter and length of the capacitor under study are 17.77 mm and 53 mm, respectively.

Figure 6: Pictorial view of the 10 μF FPE capacitors (packaged and unpackaged)

The electrical parameters for the unpackaged 10 μF capacitor, with copper tape shroud, were measured as a function of frequency using an LCR meter and the results are shown in Figures 7, 8, and 9. Measured ESR as a function of frequency, shown in Figure 7, indicates a 1 MHz value of 143 mΩ. The plot of reactance shown in Figure 8 reflects a relatively low value of ESL for the FPE capacitor. The ~900 kHz resonant frequency seen from the data of Figure 9 corresponds to an ESL of 2.72 nH. This compares very favorably to the predicted ESL finite element simulation value of 2.80 nH with a corresponding resonance of 887 kHz.

The thermal characteristics of the FPE capacitor were subsequently studied. For experimental comparison, the unpackaged FPE capacitor of Figure 6 was encased in an aluminum metal shroud and two thermocouples were used to monitor the temperature. One thermocouple was placed inside the shroud at the middle of the film and the other was placed on the outer surface. The ambient temperature was maintained at 300 K for this experimentation. Figure 10 shows the (unpackaged)

FPE capacitor inside the metal shroud along with the thermocouples.

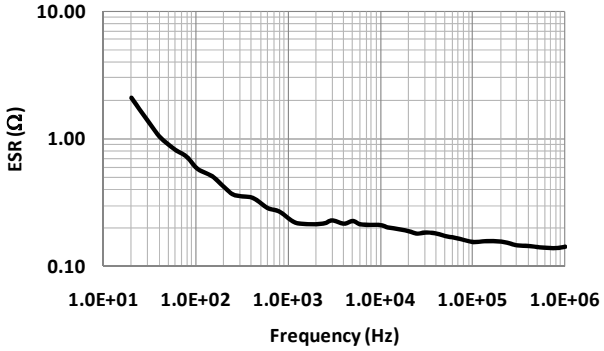


Figure 7: ESR versus frequency of the FPE capacitor.

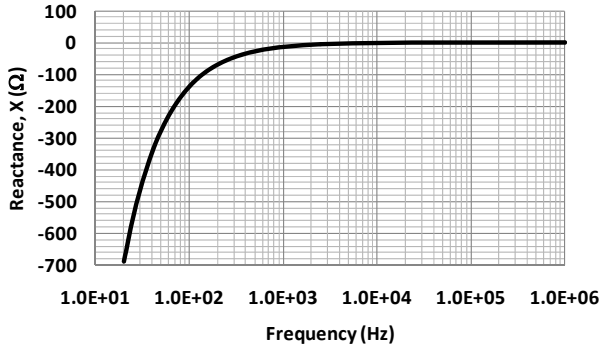


Figure 8: Reactance versus frequency of the FPE capacitor.

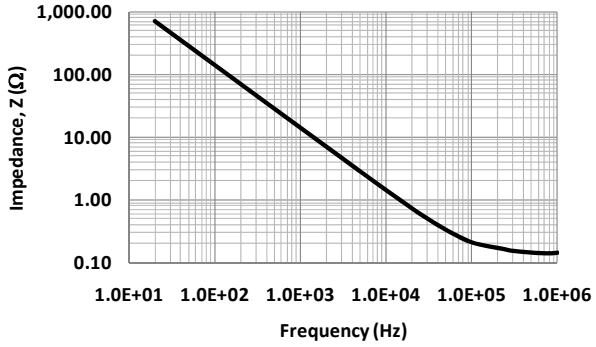


Figure 9: Impedance versus frequency of the FPE capacitor.

In conjunction with the experiment, a finite element simulation of the FPE capacitor geometry was conducted to study the temperature rise associated with 1 W of power dissipation using T=300 K as the outer surface temperature boundary condition and varying the FPE film thermal conductivity. The results of these simulations are shown in Figure 11 with temperature rise as a function of thermal conductivity. From this data a temperature rise of 10 K is predicted for the reported FPE thermal conductivity of ~0.15 W/mK.

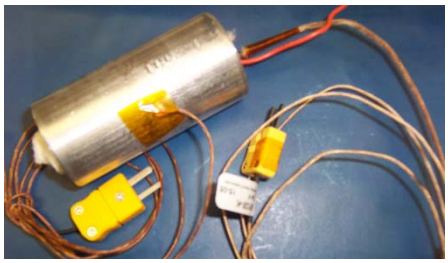


Figure 10: Pictorial view of the FPE capacitor showing the metal shroud and thermocouple locations.

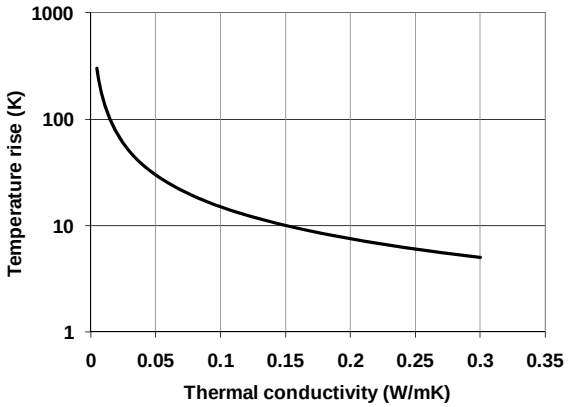


Figure 11: Simulated temperature rise as a function of thermal conductivity for 1 W of power dissipation.

The thermal conductivity of FPE film is specified as 0.13 - 0.15 W/mK [16]. However, the effective thermal conductivity of the rolled capacitor is expected to be slightly higher than 0.15 W/mK due to the insertion of fillers into the FPE polymer matrix and the presence of aluminum electrodes. Previous studies have shown that the addition of fillers in polymer systems increases the thermal conductivity of the composite [17, 18], which is the case for FPE. In order to investigate the thermal performance of the capacitor, the simulated temperature rise data was plotted as a function of power dissipation for thermal conductivities in the 0.15-0.18 W/mK range. As shown in Figure 12, the simulated data is then compared to the experimental data generated on a 10 μF FPE capacitor at three different power dissipation levels. From the empirical and predicted data an effective thermal conductivity of the FPE capacitor is found to be approximately 0.16 W/mK.

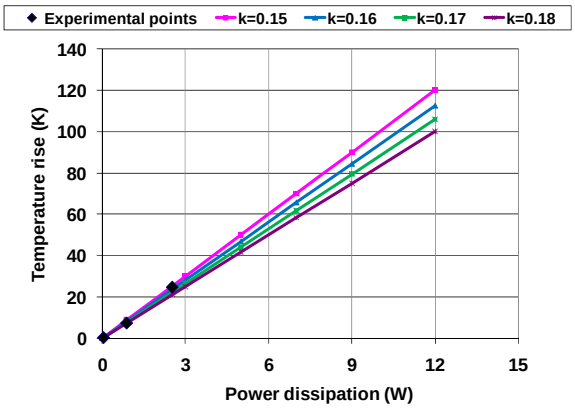


Figure 12: Simulated and experimental temperature rise versus power loss.

V. Effect of ESR on Capacitor Power Loss and Temperature Rise, and Output Voltage Ripple in a DC/DC Converter Application

The ESR effect of a filtering capacitor on the output ripple voltage of dc/dc converters is considered next. Power dissipation in capacitors due to the ac current through it and the associated temperature rise are also discussed. Figure 13 shows an inverse-coupled two-phase interleaved dc/dc boost converter suitable for high performance and high power applications [19]. A 100 V/270 V, 10 kW boost converter with a duty ratio of 0.67 and a switch frequency of approximately 75 kHz is considered for evaluating the effects of an output filter capacitor's (C_{out}) ESR on the converter output ripple voltage and capacitor power loss and temperature rise.

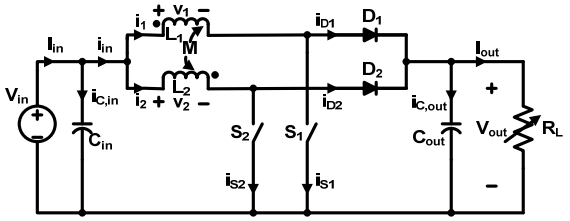


Figure 13: Circuit schematic of an inverse-coupled two-phase interleaved dc/dc converter.

For evaluating capacitor performance, the output filter is implemented using four 10 μF FPE capacitors of the type discussed in the previous section. Since the interleaved converter is two phase, the frequency which the capacitor sees is 150 kHz and, from Figure 7 data, the corresponding ESR is 158 mΩ. Using SPICE simulation, the associated current through each of the four output capacitors is shown in Figure 14. Also, the power dissipation in each of the four output capacitors and the converter's peak-to-peak output voltage ripple as a function of ESR are shown in Figures 15 and 16, respectively.

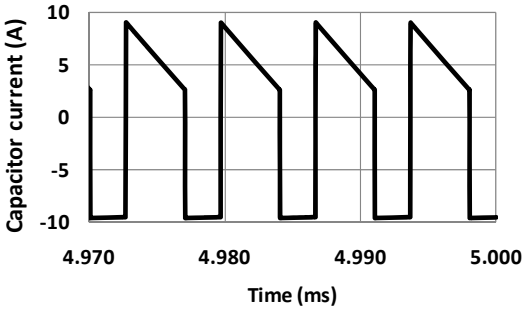


Figure 14: Individual capacitor current in a 100 V /270 V, 10 kW, 75 kHz interleaved dc/dc converter.

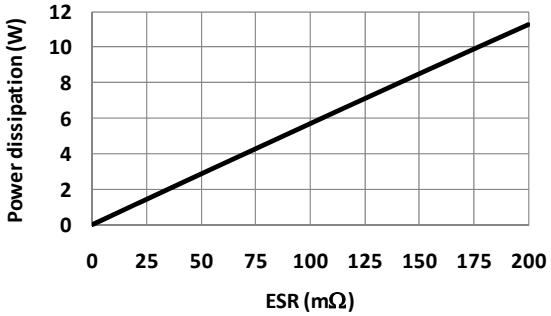


Figure 15: Power dissipation in an individual capacitor as a function of its ESR.

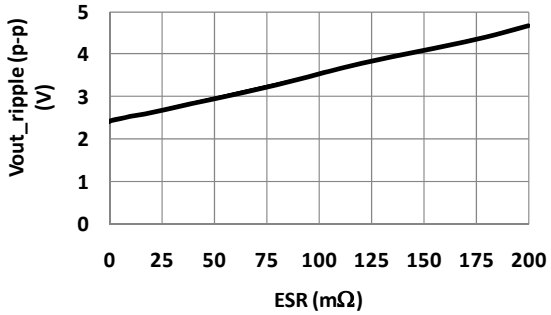


Figure 16: Output voltage ripple of a 100 V/270 V, 10 kW, 75 kHz interleaved dc/dc converter as a function of capacitor ESR.

As expected, power dissipation in the capacitor increases linearly with ESR since the converter operation is unchanged in terms of voltage and power levels. The output ripple voltage on the other hand is contributed primarily by the *ampere×second* product of the current through the capacitor and secondarily by the voltage drop in the capacitor due to ESR. It can be seen from Figure 16 that as the ESR of the capacitor gets closer to 200 mΩ, the ripple contribution due to the *ampere×second* product and the ESR become comparable.

The prediction of capacitor temperature rise using data obtained analogously to that in Figures 7, 12, and 15 can now be accomplished systematically. For example, using the data of Figure 7 for an FPE capacitor operating at 150 kHz, ESR is seen to be 158 mΩ. Using the SPICE modeled data of Figure 15, the power dissipation in the capacitor is seen to be ~9 W. The corresponding temperature rise from Figure 12 is then predicted to be 83 K. The methodology presented herein for reliably estimating temperature rise is supported by the concurrence of the experimental temperature measurements shown as the three discrete points in Figure 12. Finally, using Figure 16, the peak-to-peak output voltage ripple of the dc/dc converter is predicted to be ~ 4.2 V for a 270 V dc output for this capacitor. This corresponds to an output ripple voltage of 1.56%, which exceeds the typical converter requirement of 1%. Thus, the analysis outlined above also demonstrates the importance of a low ESR capacitor design for high power and high temperature applications.

VI. Conclusions

Using modeling and simulation, an accurate estimate of a capacitor's equivalent series inductance and temperature rise were achieved and experimentally verified using an FPE capacitor. Various architectures such as stacked, cylindrical, collapsed, and wider stacked were studied with simulation results indicating that the wider stacked architecture is superior in terms of minimizing ESL and temperature rise. A methodology to evaluate the electrical and thermal performance of a capacitor in a dc/dc converter application using both finite element analysis and SPICE simulation packages is established. The importance of a low ESR capacitor design is highlighted for a high temperature, high power and high performance dc/dc power converter application. Using the tools presented in this paper, it is possible to predict how a capacitor will perform thermally and electrically within a power converter system.

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